Remarks/Arguments

Applicant thanks the Examiner for careful consideration of the application.

Applicants amend claims 6, 30, and 33-34.

Applicants have added new claim 59.

Applicants cancel claim 31 without prejudice, and its content reserved for inclusion in a continuation/divisional application.

No claims have been allowed by the Examiner.

I. Election/Restriction:

Applicants acknowledge that Examiner has treated Applicants Election of Species IV as an election without traverse. However, Applicants traverse Examiner's statement that there is no generic or linking claim. Applicants noted in their response to the restriction response that upon allowance of a generic claim, Applicants will be entitled to consideration of claims to additional species as provided by 37 C.F.R. §1.141. Thus, Applicants assert that claims 7-9, 14, 22-29, and 57 are dependent upon independent claim 5 which if allowed would make claims 7-9, 14, 22-29, and 57 allowable. In addition, Applicants assert that if withdrawn claim 30 is presented, prior to final rejection or allowance, which ever is earlier, withdrawn claim 30 should be rejoined as a matter of right if it includes all the limitations of an another allowable product claim. Therefore, Applicants have not canceled the non-elected claims to species that arguably may still be allowable.

II. Specification Objections:

Applicants are unsure what Examiner means in referring to text on Page 1 line 1. Although Applicants in the Preliminary Amendment, submitted with this divisional application, amended the specification Applicants are unaware of any wording that

appears on Page 1 line 1. Applicants note that the amendments to the specification began with the addition of new paragraph [0010a] a figure caption.

In this response Applicants have added the new heading and paragraph after the title:

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a divisional application and claims the benefit and priority of U. S. Patent Application Serial No. 10/256,984 filed September 27, 2002 no U.S. Patent No. 6,762,094.

In addition, Examiner has objected to the title of the invention as not being descriptive. Applicants traverse this statement and believe the title as originally submitted is descriptive of the invention. However, in the interest of furthering prosecution Applicants have amended the title to read SEMICONDUCTOR DEVICES HAVING A NANOMETER SCALE JUNCTION. If Examiner continues to believe that this title is not descriptive Applicants respectfully request that Examiner provide some indication of a title that would be descriptive.

III. Rejections under 35 U.S.C. §102/103:

Examiner, on page 2 of the Office Communication appears to be asserting that claims 5, 32, and 33 are "product by process" claims. Applicants respectfully disagree with such an interpretation. Independent claim 5 reads "[a] semiconductor device, comprising: a substrate; a base epitaxial semiconducting layer including a dopant of a first polarity disposed over said substrate; a first semiconducting layer including a dopant of a second polarity disposed over said substrate; and a first junction formed between said base epitaxial semiconducting layer and said first semiconducting layer, said first junction having an area with at least one lateral dimension less than about 75 nanometers." Applicants believe that when a claim is clearly an apparatus claim, as claim 5, Examiner must specifically point out what language in the above claim Examiner is interpreting as process limitations, and provide a reasoned argument how that language would be reasonably interpreted by one of ordinary skill in the art as a process limitation. Thus, Applicants respectfully request that Examiner specifically

point the particular language Examiner interprets as process limitations and that Examiner provide a reasoned argument why such language constitutes a process limitation. In addition, Applicants believe that it is possible for words of an element or limitation to connote both a structural characteristic of a product and they can also connote a process characteristic of a method of making. However, Applicants believe that when this occurs Examiner should by default interpret those elements or limitations in there structural sense, unless the applicant has demonstrated otherwise. Further, Applicants also believe that the mere appearance of a process limitation in a claim does not convert the claim to a product by process claim. Applicants further believe that in order for a claim to be considered a product-by-process claim, each of the following elements must apply:

1. The claim must be for a product.
2. The claim must include limitations that are procedural and not structural.
3. The process limitations must describe the making of the product, not how the product is used.
4. The process limitations must be significant to the definition or description of the product.

Finally, Applicants traverse Examiner's statement that "Applicant has [the] burden of proof in such cases as the above case law makes clear." Although Applicants do not disagree that upon the making of a prima facie case of obviousness the burden shifts to the Applicant to show an unobvious difference, Applicants assert that Examiner must still make out a case of prima facie obviousness. Applicants note that MPEP 2113 states the Patent Office bears a lesser burden of proof in making out a case of prima facie obviousness for product by process claims. However, the MPEP goes on to state "[o]nce the examiner provides a rationale tending to show that the claimed product appears to be the same or similar to that of the prior art, ..." Thus, Applicants believe that Examiner must both provide a rationale how a claim is a product-by-process as well as provide a rationale how the claimed product appears to be the same or similar as the prior art of record. Both of these rationales are missing in the Office Communication.

On page 4 of the Office Communication Examiner has rejected claims 5, 6, 10-13, 15-21, 32-34 and 58 under 35 U.S.C. §102(e) as being anticipated by Lieber et al.

(U.S. Patent Publication No. 2003/0089899, "Lieber"), or in the alternative, under 35 U.S.C. §103(a) as obvious over Lieber. This rejection is respectfully traversed with regard to claims 5, 6, 10-13, 15-21, 32-34 and 58 because all of the elements of the claimed invention are not present in the cited reference.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *MPEP 2131.* The identical invention must be shown in as complete detail as is contained in the . . . claim. MPEP 2131 citing *Richardson v. Suzuki Motor Co., 868 F.2d 1226 (Fed. Cir. 1990).*

Independent claim 5 discloses "[a] semiconductor device, comprising: a substrate; a base epitaxial semiconducting layer including a dopant of a first polarity disposed over said substrate; a first semiconducting layer including a dopant of a second polarity disposed over said substrate; and a first junction formed between said base epitaxial semiconducting layer and said first semiconducting layer, said first junction having an area with at least one lateral dimension less than about 75 nanometers."

In rejecting claims 5, 6, 10-13, 15-21, 32-34 and 58 Examiner appears to have selected various claim elements and limitations found in Applicants' claims and grouped them together on page 4 of the Office Communication with the assertion that Lieber discloses all aspects of the instant invention with no reasoned argument based on sound technical and scientific reasoning to support Examiner's assertion that Lieber discloses all aspects of the instant invention. Since Examiner has provided no reasoned argument, Applicants assume that Examiner may have misinterpreted a number of terms used by Applicants in the above rejected claims. Applicants will address these issues in this response.

Applicants note that claim 5 in addition to other novel and distinct elements and limitations discloses "a base epitaxial semiconducting layer including a dopant of a first polarity disposed over said substrate." Whereas in contrast, Lieber discloses in the text describing Figures 30-39 "[i]n general, arrays of NWs [e.g. nanowires] were assembled

by passing suspensions of the NWs through fluidic channel structures formed between a poly(dimethylsiloxane)(PDMS) mold and a flat substrate (FIGS. 30A and 30B)." Page 38, paragraph [0405]. In addition, Lieber further discloses, a "typical example of parallel assembly of NWs (FIG. 31A) shows that virtually all the NWs are aligned along one direction (i.e., the flow direction). Examination of the assembled NWs on larger length scales (FIG. 31B) shows that the alignment readily extends over hundreds of micrometers." Page 38, paragraph [0406]. Lieber also discloses "[s]everal types of experiments were conducted to understand factors controlling the alignment and average separation of the NWs. First, the degree of alignment can be controlled by the flow rate. With increasing flow rates, the width of the NW angular distribution with respect to the flow direction (e.g., inset FIG. 31c) significantly narrows. Page 38, paragraph [0407]. If for the moment we ignore the process aspects of Lieber's disclosure so that we do not confuse the clearly product-by-process description of Lieber with the clear product claim of the Applicants instant invention clearly Lieber discloses a semiconductor structure disposed over a substrate wherein the semiconductor structure consists of a plurality of nanowires. Applicants argue that clearly the angular distribution shown in Fig. 31C cannot be achieved by a single nanowire but instead requires a multitude or plurality of nanowires. Therefore Applicants assert that at least in regards to Figures 30-39 Lieber does not disclose, teach, or suggest "a base . . . semiconducting layer . . . disposed over said substrate," and therefore does not disclose or render obvious Applicants' independent claim 5.

In addition, still focusing on structure Applicants note that Lieber does disclose epitaxial growth, however, it is in reference to the catalyst nanocluster deposited on a substrate from which the NWs are grown. For example, Liber discloses in paragraph [0493] "[h]omoepitaxial Si--Si core shell nanoscale wires were grown by chemical vapor deposition (CVD) using silane as the silicon reactant (Fig. 75). In this example intrinsic silicon (i-Si) nanoscale wires (sic) cores were prepared by gold nanocluster directed axial growth, which yielded single crystal structures having diameters controlled by the nanocluster catalyst diameter . . . ." Thus, Lieber discloses either a semiconductor structure disposed over a substrate wherein the semiconductor structure consists of a plurality of nanowires or a single crystal semiconducting nanowire attached

to a nanocluster catalyst wherein the nanocluster catalyst is disposed over a substrate. Applicants assert that if Examiner wants to identify the substrate, as Examiner has done on page 4 of the Office Communication, as a macroscopic substrate then one clearly must identify the semiconductor structure so formed as consisting of a multitude of nanowires. In addition, Applicants note that Lieber discloses in paragraph [0370] and Fig. 23 the formation of a junction using 2 crossed nanowires to form junctions. However, Applicants assert that such a nanowire does not constitute a base epitaxial semiconducting layer and the second nanowire does not constitute a first semiconducting layer as claimed by Applicants in the instant invention.

However, if Examiner instead identifies the nanocluster as the nanowire substrate then Lieber does disclose, in paragraph [0223] that "in FIG, 73, a p/n junction was created by introducing a p-type and an n-type dopants down on a single nanoscale wire. In addition, in paragraph [0224] Liber discloses "the nanoscale wire may be doped during growth of the nanoscale wire. . . . Additionally, the dopant may be systematically altered during the growth of the nanoscale wire, for example, so that the final nanoscale wire has a first doped region comprising a first dopant and a second doped region differing in composition from the first region." Again ignoring the process aspects of Lieber's disclosure so that we do not confuse the clearly product-by-process description of Lieber with the clear product claim of the Applicants instant invention clearly Lieber discloses an epitaxial semiconductor nanowire attached to a nanocluster catalyst that includes a junction in the nanometer scale; however, clearly the epitaxial semiconductor nanowire cannot be both the base epitaxial semiconducting layer including a dopant of a first polarity disposed over said substrate and the first semiconducting layer including a dopant of a second polarity disposed over said substrate. Thus, clearly Lieber does not disclose, teach or suggest "[a] semiconductor device, comprising: a substrate; a base epitaxial semiconducting layer including a dopant of a first polarity disposed over said substrate; a first semiconducting layer including a dopant of a second polarity disposed over said substrate; and a first junction formed between said base epitaxial semiconducting layer and said first semiconducting layer, said first junction having an area with at least one lateral dimension less than about 75 nanometers."

Further, on page 5 of the Office Communication Examiner states "how the lines are formed, either epitaxial or some other means, pertains to intermediate process steps which do not affect the final device structure." Applicants argue that epitaxial is not a process but rather clearly denotes structural characteristics, i.e. crystallographic structure. Examiner has provided no reasoned argument based on sound technical and scientific reasoning to support Examiner's assertion that epitaxial is a process and does not include any structural characteristics. Applicants respectfully request that Examiner provide a reasoned argument how epitaxial is only a process and not structure if Examiner so continues to assert.

Because Lieber does not disclose "[a] semiconductor device, comprising: a substrate; a base epitaxial semiconducting layer including a dopant of a first polarity disposed over said substrate; a first semiconducting layer including a dopant of a second polarity disposed over said substrate; and a first junction formed between said base epitaxial semiconducting layer and said first semiconducting layer, said first junction having an area with at least one lateral dimension less than about 75 nanometers," as recited in independent claim 5, Lieber does not anticipate or render obvious independent claim 5, since the above elements of the instant claimed invention are arranged in a manner distinct from that disclosed in Lieber.

Since a proper anticipation rejection requires that there be present in a single prior art reference a disclosure of all of the elements of the claimed invention arranged as in the claims, Applicants believe that Lieber does not anticipate the present invention. *See* MPEP 2131. Applicants note independent claim 32 has similar limitations as independent claim 1 that Lieber also does not anticipate. In addition, Applicants have also amended claim 30 to include all of the limitations of claim 5 and therefore believe that withdrawn claim 30 is allowable and is not anticipated by Lieber. Therefore, Applicants respectfully request that the Examiner withdraw the rejection of claims 5, 6, 10-13, 15-21, 32, and 58 based on Lieber under 35 U.S.C. § 102(e).

Dependent claims 5, 6, 10-13, 15-21 are dependent upon independent claim 5, and are therefore believed to be allowable, at least for this reason alone, as dependent upon a believed allowable claim. Accordingly, Applicants believe that the rejection of claims 5, 6, 10-13, 15-21 has been overcome. Therefore, Applicants respectfully request that the Examiner withdraw the rejection of dependent claims 5, 6, 10-13, 15-21 under 35 U.S.C. § 102(e) in respect to Lieber.

In addition, in regards to amended independent claim 33, claim 33 discloses, a "semiconductor device, comprising: a substrate; an epitaxial semiconducting structure disposed on said substrate; a polycrystalline semiconducting structure disposed over said substrate; and means for rectifying current disposed between said epitaxial semiconductor structure and said polycrystalline semiconducting structure, said means for rectifying current having an area with at least one lateral dimension less than about 75 nanometers. As argued above for independent claim 5 Lieber does not disclose an epitaxial semiconducting structure disposed on said substrate, does not disclose a polycrystalline semiconducting structure disposed over said substrate, and means for controlling current flow disposed between said epitaxial semiconductor structure and said polycrystalline semiconducting structure, said means for controlling current flow having an area with at least one lateral dimension less than about 75 nanometers. Accordingly, Applicants believe that the rejection of claims 33-34 has been overcome. Therefore, Applicants respectfully request that the Examiner withdraw the rejection of dependent claims 33-34 under 35 U.S.C. § 102(e) in respect to Lieber.

In regards amended dependent claim 6, claim 6 discloses "a second semiconducting layer including a dopant of said second polarity disposed over said base epitaxial semiconducting layer; and a second junction disposed between said epitaxial semiconducting base layer and said second semiconducting layer having a length and a width, and said second junction having an area with at least one lateral dimension less than about 75 nanometers. As previously argued above for independent claim 5 Applicants assert that a nanowire is not a layer. Accordingly, Applicants believe that the rejection of amended dependent claim 6 has been overcome. Therefore, Applicants

respectfully request that the Examiner withdraw the rejection of amended dependent claim 6 under 35 U.S.C. § 102(e) in respect to Lieber.

In regards dependent claim 10, claim 10 discloses "wherein said substrate further comprises a semiconductor substrate having a dopant of said second polarity, wherein said semiconductor substrate forms said first semiconductor layer." Applicants have been unable to find where Lieber discloses "wherein said semiconductor substrate forms said first semiconductor layer," that is where Lieber discloses a junction formed between the substrate and the base epitaxial semiconducting layer. Applicants respectfully request that Examiner particular point our where in Lieber such a disclosure is made. Accordingly, Applicants believe that the rejection of dependent claim 10 has been overcome. Therefore, Applicants respectfully request that the Examiner withdraw the rejection of dependent claim 10 under 35 U.S.C. § 102(e) in respect to Lieber.

In regards dependent claim 11, claim 11 discloses "wherein said base epitaxial semiconducting layer further comprises a plurality of epitaxial semiconducting base lines substantially parallel to each other, and said first semiconducting layer further comprises a plurality of first semiconducting lines substantially parallel to each other and at a predetermined angle to said plurality of epitaxial semiconducting base lines." Similar to the arguments made above Applicants believe that Lieber does not disclose a base epitaxial semiconducting layer and does not disclose a first semiconducting layer therefore Lieber does not disclose a plurality of epitaxial semiconducting base lines and does not disclose a plurality of first semiconducting lines. Accordingly, Applicants believe that the rejection of dependent claim 11 has been overcome. Therefore, Applicants respectfully request that the Examiner withdraw the rejection of dependent claim 11 under 35 U.S.C. § 102(e) in respect to Lieber.

In regards dependent claim 12, claim 12 discloses "a plurality of second semiconducting lines substantially parallel to each other and at a predetermined angle to said plurality of epitaxial semiconducting base lines." Applicants have been unable to find where Lieber discloses " a plurality of second semiconducting lines substantially parallel to each other and at a predetermined angle to said plurality of epitaxial

semiconducting base lines," that is where Lieber discloses three sets of lines. Applicants respectfully request that Examiner particular point our where in Lieber such a disclosure is made. Accordingly, Applicants believe that the rejection of dependent claim 12 has been overcome. Therefore, Applicants respectfully request that the Examiner withdraw the rejection of dependent claim 12 under 35 U.S.C. § 102(e) in respect to Lieber.

In regards to Examiner's rejection of claims 5, 6, 10-13, 15-21, 32-34 and 58 under 35 U.S.C. §103(a) Applicants believe this rejection has been overcome because Applicants have argued that Lieber is not a proper anticipation rejection and that claims 5, 6, 10-13, 15-21, 32-34 and 58 are not product-by-process claims. Applicants believe if Examiner maintains the single reference 103 obvious rejection that Examiner must be relying on Examiner's own knowledge. Since Examiner has not provided a reasoned explanation of how each of the limitations or group of limitations as claimed subject matter of claims 5, 6, 10-13, 15-21, 32-34 and 58 is obvious in view of Lieber. Thus, at this time Applicants request under 37 C.F.R. §1.104(d)(2) that if Examiner is relying on personal knowledge then Examiner should provide an affidavit with specific factual findings predicated on sound technical and scientific reasoning, that it would have been obvious at the time the invention was made, to a person having ordinary skill in the art, to modify the invention of Lieber so that Lieber would have the claimed limitations set out in claims 5, 6, 10-13, 15-21, 32-34 and 58.

In regards to independent claim 1, Examiner has rejected claim 1 under 35 U.S.C. §103(a) as being unpatentable over Lieber et al. in view of Kitamura (JP abstract 59-106147, "Kitamura"). This rejection is respectfully traversed with regard to claim 1 since neither Lieber nor Kitamura, taken either individually, or in combination therewith, teach, suggest, or mention the claimed invention.

To establish a prima facie case of obviousness, three basic criteria must be met. There must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, i.e. the prior art must suggest the desirability of the claimed invention. There must be a reasonable

expectation of success. Finally all claim limitations must be taught or suggested by the prior art. MPEP §2143. These requirements are not met here.

Claim 1 discloses a "semiconductor device, comprising: a substrate including a dopant of a first polarity; a first semiconducting structure including a dopant of a second polarity and disposed over said substrate, said first semiconducting structure having substantially planar top and side surfaces; a first junction formed between said first semiconducting structure and said substrate, said first junction having an area with at least one lateral dimension less than about 75 nanometers." Examiner admits Lieber does not disclose wherein the first semiconducting structure has substantially planar top and side surfaces. Examiner asserts that Kitamura teaches a first semiconductor structure having planar top and side surfaces. Applicants respectfully request that Examiner provide a full translation of this Japanese Patent since it is unclear with the abstract alone exactly what Kitamura discloses. Applicants note that Kitamura discloses "a plurality of polycrystalline silicon layer belts and a plurality of conductive layer belts which are orthogonally crossing through an insulating film, providing contacts to the intersecting points . . . ." Applicants further note Kitamura discloses "the silicon layer 11 becomes open since contact does not exist at the position of bit B2 . . . ." Without a full translation Applicants assert that neither Applicants nor Examiner can fully understand the disclosure of Kitamura and its teachings, suggestions, and motivations. In addition, Applicants argue that the abstract of Kitamura does not disclose, teach, or suggest using nanowire structures as disclosed in Lieber or provide any motivation to modify Lieber. In fact Applicants argue that Kitamura teaches away from Lieber. Kitamura at best appears to possibly suggest using conventional lithography and etching techniques to form the semiconductor structures shown in Kitamura. Applicants are unsure without the full translation, but note that Kitamura may be written to a mask for ROM structures. Lieber on the other hand never suggests nor mentions, convention lithography and etching techniques to form the nanowires described in Lieber. Applicants assert that this is supported by Lieber since Lieber discloses, in paragraph [0220] "the memory switching devices may be assembled specifically from nanoscale material building blocks **and may not be created in planar materials by lithography**," clearly teaching away from Kitamura. Thus, Applicants assert that

without a full translation Examiner has simply taken a figure out of context to the specification and has provided no reasoned argument based on the entire specification that is required to establish a prima facie case of obviousness. Accordingly, Applicants believe that the rejection of independent claim 1 has been overcome. Therefore, Applicants respectfully request that the Examiner withdraw the rejection of independent claim 1 under 35 U.S.C. § 103(a) in respect to Lieber in view of Kitamura.

In regards to dependent claims 2-4 Applicants note that at least with the arguments presented above Lieber and Kitamura do not show most aspects of Applicants claimed invention and therefore the rejection of claims 2-4 as being unpatenable over Lieber in view of Kitamura and further in view of Taussig has been overcome. In addition, Applicants argue that Figures 23-25 do not show "a second semiconducting structure including a dopant of said first polarity formed on said first semiconducting structure said second semiconducting structure having substantially planar top and side surfaces; and a second junction formed between said first semiconducting structure and said second semiconducting structure, said second junction having a length and a width, and said second junction having an area with at least one lateral dimension less than about 75 nanometers," as claimed by Applicants. Applicants note that Figures 23-25 show electrically conductive lines 808 and 812 with a semiconductor layer deposited oover the first conductor arrangement on the substrate 806 of the first sub-layer 802. Col. 21, 33-36. Accordingly, Applicants believe that the rejection of dependent claims 2-4 has been overcome. Therefore, Applicants respectfully request that the Examiner withdraw the rejection of dependent claims 2-4 under 35 U.S.C. § 103(a) in respect to Lieber in view of Kitamura and further in view of Taussig.

Therefore, in view of the foregoing Amendment and Remarks, Applicants believe the present application to be in a condition suitable for allowance. Examiner is respectfully urged to withdraw the rejections, reconsider the present Application in light of the foregoing Amendment, and pass the amended Application to allowance.

If the Examiner has any questions, or if a telephone interview would in any way advance prosecution of the application, the Examiner is respectfully requested to call Applicants' representative at (541) 715-1694 to discuss the steps necessary for placing the application in condition for allowance.

Favorable action by the Examiner is solicited.

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Date: 3-Feb-06